Notice of Allowability	Application No.	Applicant(s)	
	09/943,595	SWOBODA, GARY L.	
	Examiner	Art Unit	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 7/5/07.

2. ☒ The allowed claim(s) is/are 1-4,16,17 and 27-54.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

FRED FERRIS
PRIMARY EXAMINER
TECHNOLOGY CENTER 2100

DETAILED ACTION

1. Claim(s) 1-4, 16-17, 27-54 has/have been presented for examination based on amendment filed on 5th July 2007.
2. Claim(s) 1, 16, and 27 is/are amended.
3. The arguments submitted by the applicant have been fully considered.
4. Examiner withdraws the rejection made under 35 USC 101 as the data is now transmitted from data processor integrated circuit to a external host and data being transmitted is second information block.
5. Examiner also withdraws the rejection made under 35 USC 103 in view of applicant's amendment.
6. This office action also contains an *Examiner's Amendment* to the specification.
7. Claims 1-4, 16-17, 27-54 are now allowable. Please see reasons for allowance below.

EXAMINER'S AMENDMENT

7. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

Changes are made to the specification, "BREIF DESCRIPTION OF THE DRAWINGS" section, Pg. 10 Lines 13-14, to appropriately present reference to and brief description of the drawing(s) as set forth in 37 CFR 1.74.

Modification made to the Pg.10 Lines 13-14 as follows:

FIGURES [[23-27]] 23, 23A and 23B illustrate exemplary operations which can be performed by the transmission formatter of FIGURES 22 and FIGURE 22A.

New additions made to the Specification Pg.10 on Lines 15-16 as follows:

FIGURES 24-27 illustrate exemplary operations which can be performed by the transmission formatter of FIGURES 22 and FIGURE 22A.

Allowable Subject Matter

8. The following is a statement of reasons for the indication of allowable subject matter:

Regarding Claim 1

Claim 1 discloses a method of exporting emulation information from a data processor integrated circuit. Almost all the limitations are taught by the prior art of record (Edwards in view of Baird), except the argued/amended limitations

> "arranging the collected emulation information into a plurality of first information blocks organized in a sequence, each of said first information blocks having a first fixed size, wherein each of a plurality of consecutive ones of said first information blocks contains a constituent bit of a multi-bit signal used by the data processor;
> receiving the plurality of first information blocks and arranging the emulation information contained therein into a plurality of second information blocks organized in a sequence, each of said second information blocks having a second fixed size which differs from the first fixed size of the first information blocks, wherein each of a contains a constituent bit of said multi-bit signal;"

Support for limitation is present in specification Fig.9 and Fig.23-23B.

U.S. Patent No 6,732,307 issued to Edwards teaches first information block and then arranging into second information blocks (Edwards: Col. 2, Lines 31-33; *Col.1 Line 13-14 – SOC, 56-57- ICE;* Col. 17, Lines 45-52 in trace buffer 227; Col. 7, Lines 27-31; Fig.2, Element 202; Fig 11A &11B; Col.19 Lines 3-19*)*, however lacks the format of the "first information blocks contains a constituent bit of a multi-bit signal used by the data processor" as having the exact structure of packet as in Fig.9 and further lacks arranging into second information blocks in form of exact bit pattern as shown in specification Fig.23-23B specifically (packets converted from 10 bits to 6 bits, 10 bits to 12 bits, 10 bits to 16 bits).

U.S. Patent No. 5,848,264 issued to Baird et al teaches first information blocks organized in a sequence as coming in the debug queue in a FIFO memory (First in

First out) (Baird: Col.3 Lines 37-44) having a consecutive number of first information blocks indicated by timestamp (Baird: Col.3 Lines 53-56) which defines the consecutive bits of emulation information sent to the external system. The first fixed size could be 16, 32 or 64 bits dictated by level of detail needed to be captured (Baird: Col.5 Lines 59-Col.6 Lines 3).

Further Baird teaches receiving plurality of first information blocks from the FIFO debug queue and second information blocks organized into sequence where the second fixed size is limited by number of pins going to external system (Baird: Col.10 Lines 41-53). The second fixed size, 16 bits differs from the first fixed size of 32 and 64 bits. The information is offloaded sequentially as the memory the debug information is held is FIFO (Baird: Col.3 Lines 37-44). Further Baird teaches, wherein *said second number differs from said first number*... (Baird: Col.11 Lines 5-43). Baird however lacks the format of the "first information blocks contains a constituent bit of a multi-bit signal used by the data processor" as having the exact structure of packet as in Fig.9 and further lacks arranging into second information blocks in form of exact bit pattern as shown in specification Fig.23-23B specifically (packets converted from 10 bits to 6 bits, 10 bits to 12 bits, 10 bits to 16 bits) as well.

U.S. Patent No. 6,229,808 issued to Teich et al teaches a first fixed size (Teich: Fig.9 ATM Cells) is an integral multiple of second fixed size (Teich: Fig.9 Local Data Package). The selecting and arranging is obvious in the design as for conversion between ATM package and Local package (Teich: Fig.9; Col.5 Lines 50-Col.6Lines21) would necessitate the need for selecting bits. However this

implementation is in form of ATM packets and is not happening inside a data processor integrated circuit as disclosed (See Fig.1).

U.S. Patent No. 5,953,339 issued to Baldwin al teaches a first fixed size (Baldwin: Fig.1 LLC packets) is a forming a *non-integral multiple of second fixed size* (Baldwin: Fig.1 ATM packets). The selecting and arranging is obvious in the design as for conversion between ATM packets and LLC packets (Baldwin: Fig.9; Col.5 Lines 50-Col.6Lines21) would necessitate the need for selecting bits and remembering last LLC packet bits. However this also implementation is in form of ATM packets and is not happening inside a data processor integrated circuit as disclosed (See specification Fig.1).

U.S. Patent No. 5,790,398 issued to Horie teaches use of NOP bits as pseudo-transmission data transmission, indicating that no data is being transmitted and for synchronization purpose (Horie: Fig.3C; Col.6 Lines 25-34). It would be obvious to use the NOP when no data is present to be transmitted from the teachings of Horie and initializing the NOP bits in first information block. However Horie is not related to exporting emulating information.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 9:30 - 6:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Friday, July 27, 2007

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